A LOW NOISE, AGC SILICON TRANSISTOR USEFUL FROM LF TO UHF

by David Bingham, Harry Suzuki, and Charles Watson

INTRODUCTION

Approximately a year and a half ago, the 0045 project was initiated at the Fairchild Research and Development Laboratories. At the time, there was a definite need for a silicon transistor which would give useful unneutralized power gains at the i-f frequencies and high power gains and low noise figures at the VHF and UHF frequencies.

The most important parameters to be considered for a device of this type are: a low r_b' which is essential for low noise figures, a low reverse capacitance for high stable gains, and a high f_t for UHF applications. An additional requirement is that the device exhibit forward Automatic Gain Control (AGC) characteristics.

DESIGN CONSIDERATIONS

The initial design criteria for 0045 was for a transistor capable of a useful power gain and low noise figure to 860 megacycles. Additionally, the power gain, noise figure, and forward AGC characteristics at VHF were not to be compromised.

To optimize r-f performance, it is necessary to maximize the ratio of emitter periphery to emitter area while maintaining a reasonable base area aspect ratio. This implies a series of very narrow emitter stripes. Diffusion of narrow emitter stripes in itself presents no great problem; however, removal of the oxide over the center of the stripe (for the aluminum contact) without exposing the base emitter junction involves close tolerances. In the case of the 0045 masking, tolerances are held to 0.1 mil allowing a 0.1 mil oxide cut to be placed over the 0.25 mil emitter stripes. The ability to mask such a cut makes possible high-volume production compatible with the above mentioned objectives.

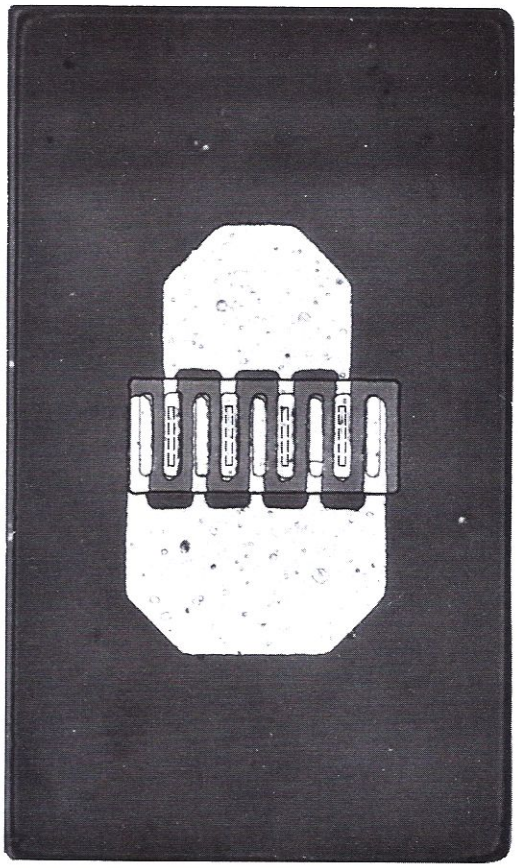


FIG. 1. Photomicrograph of 0045 chip

Figure 1 shows a photomicrograph of the 0045 chip. There are four emitter stripes and five base stripes. The spacings between stripes are 0.25 mil. For clarity, the emitter contact cutouts have been emphasized by dotted lines. The die size of 10 by 15 mils is large enough for ease of handling and power dissipation (175 mW at 25°C ambient temperature) and small enough to result in an economic yield of dice per wafer. The above tolerances also result in high yields in today's production.

COPYRIGHT, FAIRCHILD SEMICONDUCTOR, 1966 • PRINTED IN U.S.A. 2350-050-36 5M

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Fairchild cannot assume responsibility for use of any circuitry described. No circuit patent licenses are implied.

The choice of the material resistivity and its tolerance are important to guarantee the devices electrical parameters. The relative manner in which the material resistivity affects device parameters is given in Table I.

TABLE I

	High Resistivity	Low Resistivity
f_T	low	high
r_b prime	low	high
go (output conductance)	low	high
gi (input conductance)	high	low
Forward AGC characteristic	good	poor
Collector-base depletion capacity	low	high

The material resistivity found to offer the best compromise is 7 ohms/cm. This allows a good forward AGC characteristic, low collector to base depletion capacitance, and a reasonable compromise on noise figure and UHF power gain.

Because minimizing the reverse transfer capacitance was an important objective with this device, the size of the bond wire was an important consideration. The larger the diameter of the wire, the larger the pad area needed for the bond; and consequently, the larger the capacitances between the base and emitter bonding pads and the collector. Possible choices were between wedge and ball bonds with wire diameters ranging from 0.5 mil to 1 mil. Again, a compromise was made and 0.7 mil gold wire with ball bonds were selected. This increased the collector-base and collector-emitter capacitances by 0.1 pf over 0.5 mil wedge bonds; however, the higher yields and lower assembly costs were much more favorable.

PACKAGE CONSIDERATIONS

The principle package consideration is the parasitic capacitance between any two pins. In order to make full use of the small capacitances between the base and emitter and the collector, the parasitic package capacitance should not be greater than 10% of either of these capacitances. Other important considerations are the mechanical support and protection to the chip, reasonable power dissipation, minimum parasitic inductance from the lead wires between the die and inside connection to the package pins (important only at UHF), and a package conveniently used by set manufacturers.

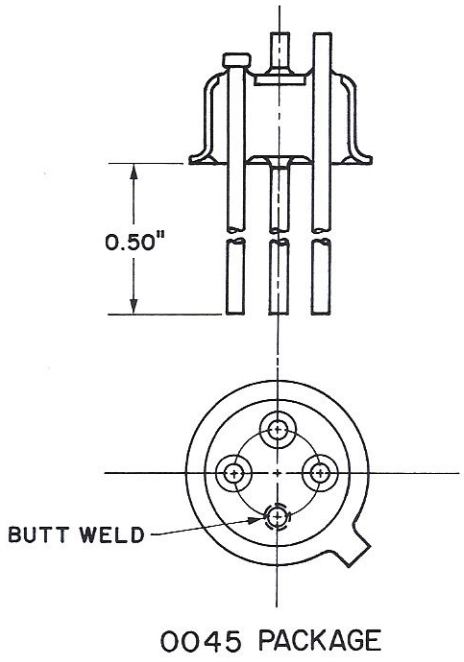


FIG. 2. Low transfer-capacitance package

Figure 2 shows the package selected which conforms to the standard TO-18 outline. The package has four half inch leads, one of which is connected to the casing. The nail-head post to which the die is connected is completely surrounded by the metal casing. Hence, the nail-head post is electrically shielded from the other two isolated posts. With the shield grounded, the capacitance between the nail-head post and either of the other two posts is under 0.035 pf.

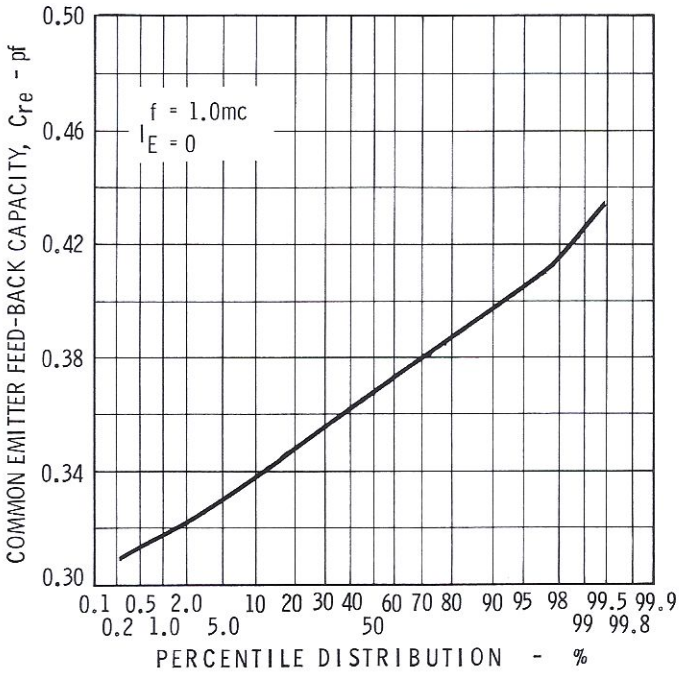


FIG. 3. Percentile distribution of C_{re}

Figure 3 shows the percentile distribution of the reverse transfer capacitance, C_{re}. As a result of minimizing this parameter, the spread of C_{re} is between 0.31 pf and 0.43 pf with the typical value 0.37 pf.

DEVICE FIGURES OF MERIT

The gain and stability figures of merit were derived from the two-port Y parameters where

Yi = gi + jbi = short circuit input admittance
Yo = go + jbo = short circuit output admittance
Yf = gf + jbf = forward transfer admittance
Yr = gr + jbr = reverse transfer admittance

$$MAG = 10 \log \frac{Y_f^2}{4gigo}$$

$$GMS = 10 \log \frac{Y_f}{Y_r}$$

$$GMA = 10 \log \frac{GMS}{k+\sqrt{k^2-1}}$$

$$k = \frac{2gigo - Re\,(Y_r\,Y_f)}{|\,Y_r\,Y_f\,|}$$

FIG. 4. Formulas for figures of merit

Figure 4 shows the expressions for the various figures of merit in terms of the Y parameters.

Maximum Available Gain

The Maximum Available Gain (MAG) can be considered a practical figure of merit for moderately high frequencies and for applications where a high degree of neutralization is obtainable. At the low frequencies, values of MAG for the 0045 are in the order of 50 db but difficult to obtain using practical circuit Q's. While MAG is a significant figure of merit, its value must be weighed against circuit complexity and ease of alignment in a practical amplifier.

Gain Maximum Stable

Gain Maximum Stable (GMS) is a somewhat more practical figure of merit for unneutralized or partially neutralized amplifiers than MAG. GMS defines the limit of gain that can be taken from a single stage without danger of oscillation. GMS quite often cannot be obtained at the higher frequencies.

k (Stability Factor)

GMS implies a certain degree of stability. Following Rollett (Ref) a device stability factor k can be defined to equal one when the gain is equal to GMS. k can assume values bounded by -1 and + infinity and is a function of the two port driving points and transfer functions.

Gain Maximum Available

Gain Maximum Available (GMA) can be expressed in terms of the Y parameters as

$$GMA = 10 \log \frac{|Y_f|^2}{2gigo - Re\left(Y_r Y_f\right) + \sqrt{\left\{\left[2gigo\,Re\left(Y_r Y_f\right)\right] - \left|Y_r Y_f\right|^2\right\}}}$$

or, expressed in terms of k and the forward to reverse ratio, as

$$GMA = 10 \log \left|\frac{Y_f}{Y_r}\right| \frac{1}{k + \sqrt{\left(k^2 - 1\right)}}$$

Hence, it can be seen that MAG, where Y_r is assumed to equal zero, and GMS, where k is assumed to equal one, are only special cases of GMA.

In the majority of cases, the designer does not utilize the full gain capabilities of the transistor as expressed in the above figures of merit. As an example, if the GMS is 30 db, $k < 1$, and the gain requirement of the stage is only 24 db, extra loading may be introduced in the form of GS (source conductance) and GL (loading conductance). A new circuit stability factor K can now be derived.

$$K = \frac{2(gi + GS)\,(go + GL) - Re\left(Y_f Y_r\right)}{\left|Y_f Y_r\right|}$$

By adding appropriate values of GS and GL, K can be forced to some value greater than 1. For this example let K = 2. Then since

$$GMS = 30 \text{ db} = 1000 = \left|\frac{Y_f}{Y_r}\right|$$

it follows that

$$GMA = 10 \log \frac{1000}{2 + \sqrt{\left(2^2 - 1\right)}} = 24.3 \text{ db}$$

Gains of this order are often referred to as MUG and a stability factor of at least S = 4 is implied, where S is inversely equal to the product of the forward voltage gain and the reverse voltage gain. In summarizing, to determine circuit power gain, MAG is of primary interest for neutralized amplifiers. For unneutralized amplifiers, GMS is used when $k < 1$, and GMA is used when $k \geq 1$.

Plots of MAG, GMS, GMA, and k are shown as functions of frequencies in Figs. 5, 6, and 7.

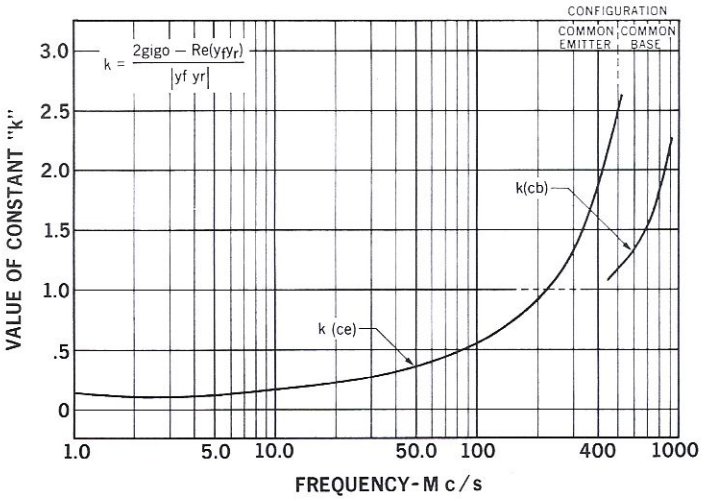


FIG. 5. Stability factor "K" versus frequency

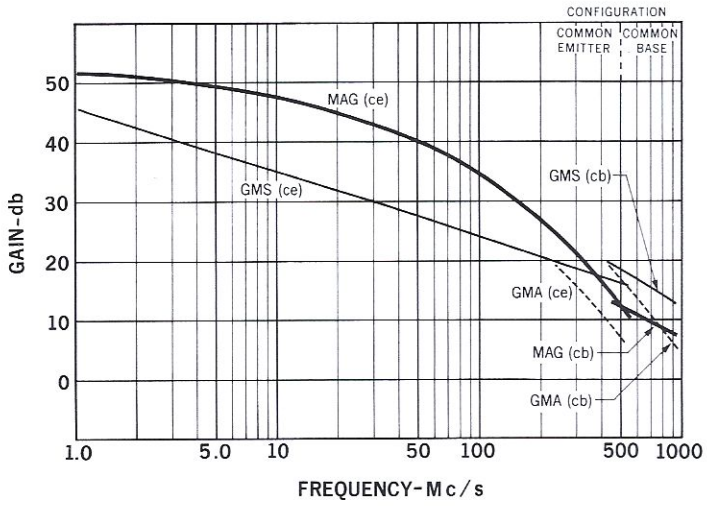


FIG. 6. MAG, GMS, and GMA versus frequency

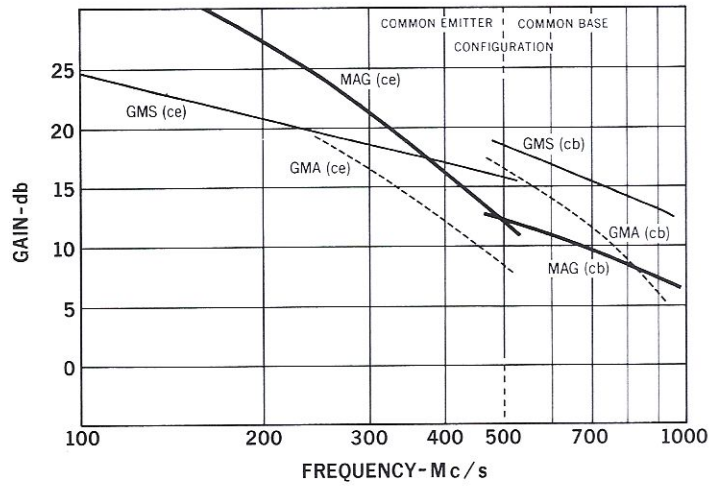


FIG. 7. MAG, GMS, and GMA versus frequency

NOISE FIGURE

Figure 8 shows a curve of noise figure versus frequency for a source admittance of 20 + j0 mmho with the device operating at 2 mA collector current and 10 volts collector-emitter. Noise figures under 2 db have been obtained at 1 megacycle with the device operating at 300 μA and 10 volts and fed from a 600 Ω source. Similarly, 2 db noise figures at 10 kilocycles were achieved with the bias at 20 μA and 10 volts and fed from a 10 KΩ source.

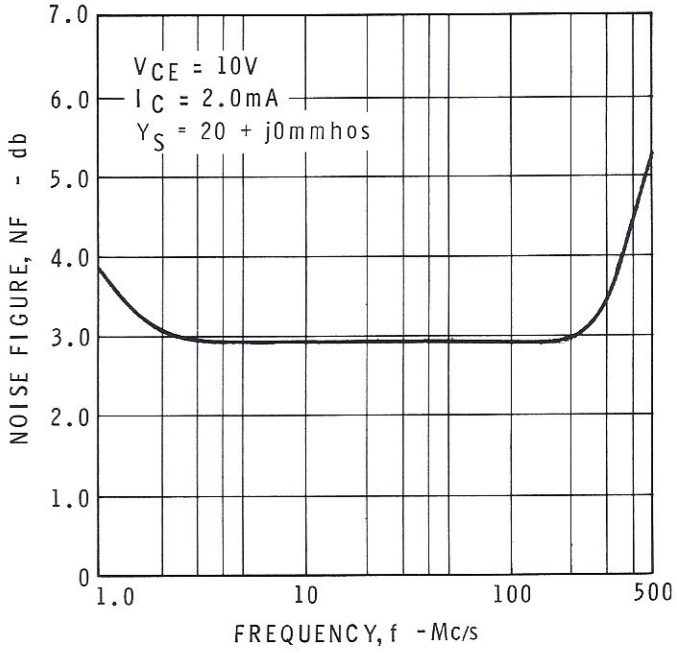
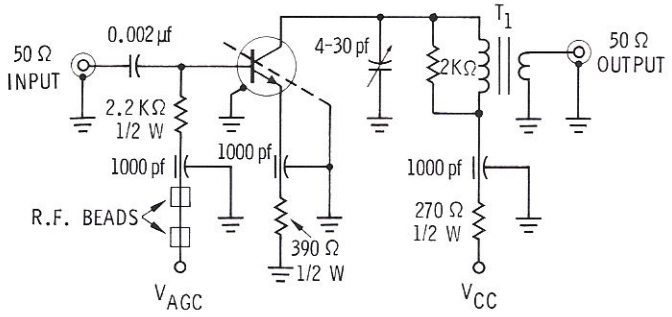


FIG. 8. Noise figure versus frequency

AGC

In order to control the gain of a stage using the 0045, the collector current may be decreased (reverse AGC) or increased (forward AGC) from the maximum gain point. The 0045 is designed to allow forward gain control of the order of 60 db at moderate collector currents. It has been found to be more practical to express the forward gain control characteristics in terms of a simulated AGC voltage, As an example, in a test circuit such as the one shown in Fig. 9, a certain class of device may be stated to have 30 db of gain reduction for a control voltage bounded by 4.4 and 5.4 volts. Another class of 0045 may be sorted in the same test circuit for 30 db of gain reduction bounded by 5.2 and 6.2 volts of control voltage. In the case of a television video i-f amplifier having two gain control stages, the above selection provides the designer with tightly controlled device spreads for each stage.



T_1 : Q_3 Toroid 4:1 Ratio } #22 Wire
8T-PRI 2T-SEC }

FIG. 9. 45 Mc/s AGC, power gain, and noise figure test fixture

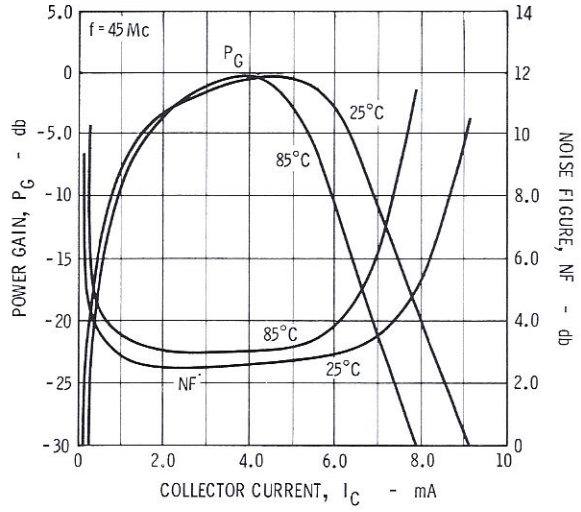


FIG. 10. Typical 45 Mc/s AGC characteristics, gain reduction versus control voltage

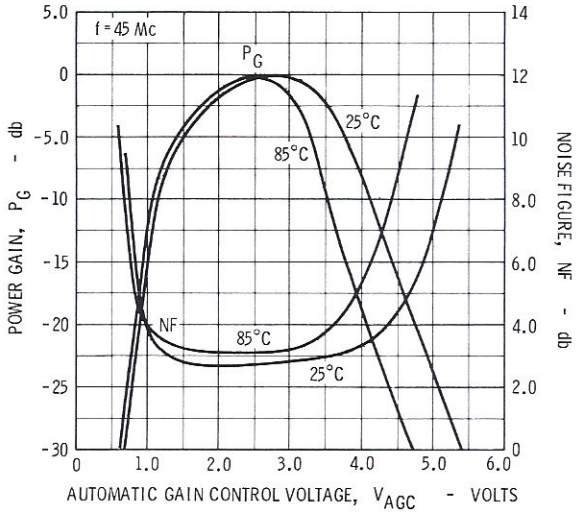
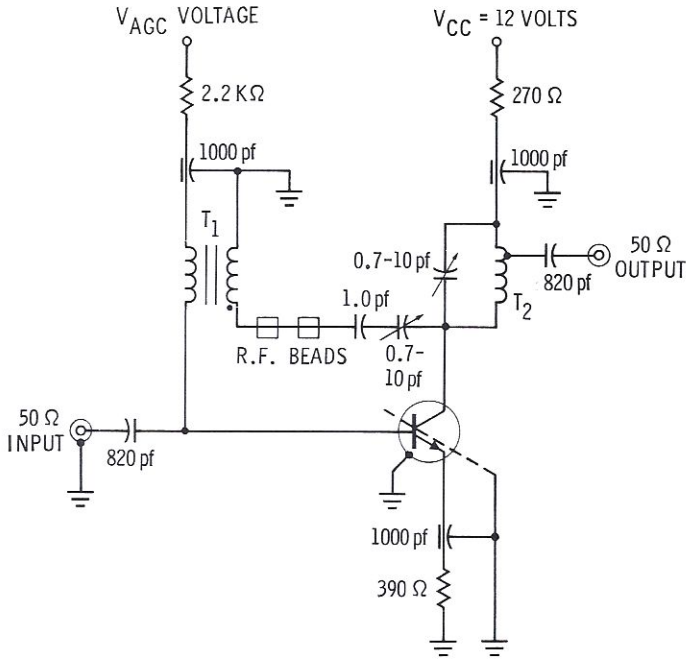


FIG. 11. Typical 45 Mc/s AGC characteristics, gain reduction versus collector current

CIRCUIT PERFORMANCE

Unneutralized gain as a function of collector current and control voltage is shown in Figs. 10 and 11. Similar characteristics are obtained in neutralized test circuits such as the 200 Mc/s amplifier shown in Fig. 12. Typical control voltages required for 30 db gain reduction at 200 Mc/s lie between 4 and 5 volts.



T_1: Ferrite Core Indiana Gen. Corp. F-684-Q_3
T_2: 6 Turns #16 Buss Wire ID= 1/4"L=3/4"

FIG. 12. 200 Mc/s AGC, power gain, and noise figure test fixture

An application of the 0045 which has not made an appearance on the U. S. scene, but is extensively used in the European market, is shown in Fig. 13. The UHF television tuner uses two 0045's in the common-base configuration. The input to the AGCable r-f amplifier is untuned, with a double-tuned interstage preceding the autodyne mixer. Figure 14 shows the typical power gain and noise figure of the tuner over the UHF television band.

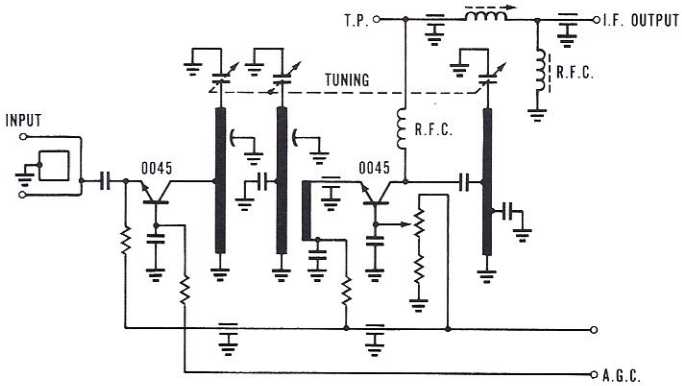


FIG. 13. European UHF tuner using forward AGC

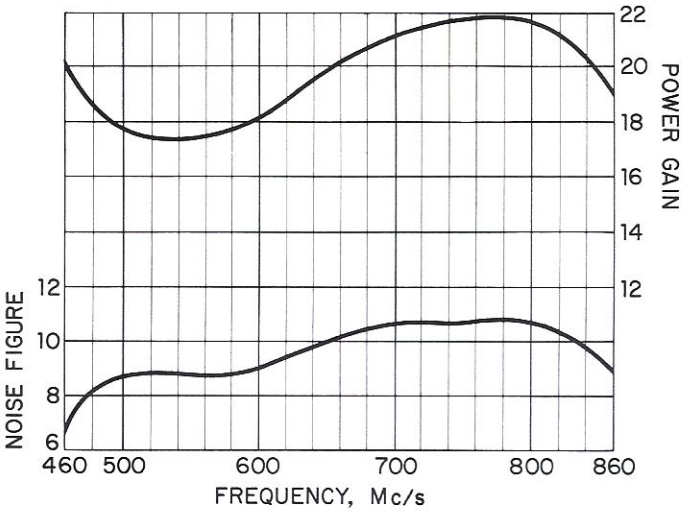


FIG. 14. Noise figure and power gain versus frequency of the UHF tuner

Table II shows the typical performance obtainable at various common frequencies.

TABLE II
TYPICAL PERFORMANCE

FREQUENCY	POWER GAIN	NOISE FIGURE	CONFIGU-RATION	NEUTRA-LIZED
455Kc/s	40 db	3.0 db	CE	NO
4.5 Mc/s	36 db	3.0 db	CE	NO
10.7 Mc/s	32 db	3.0 db	CE	NO
27 Mc/s	27 db	3.0 db	CE	NO
45 Mc/s	25 db	3.0 db	CE	NO
45 Mc/s	40 db	3.0 db	CE	YES
100 Mc/s	28 db	3.0 db	CE	YES
200Mc/s	25 db	3.0 db	CE	YES
500Mc/s	12 db	5.5 db	CB	NO
800Mc/s	9 db	8 db	CB	NO

CONCLUSION

An NPN silicon transistor optimized for a wide range of consumer small signal applications has been developed. High volume production is made possible by Fairchild's development of tenth mil technology. Careful material control and device classification make available a family of tightly controlled high quality devices.

Various figures of merit for such a device were discussed and shown as functions of frequency.

Performance in various circuits was discussed and a table of typical performance at commonly used frequencies was presented.

ACKNOWLEDGEMENT

The authors express their appreciation to Garth Mellick for the numerous measurements and gathering of data.

REFERENCE

J. M. Rollett, "Stability and Power-Gain Invariants of Linear Two-Ports," IRE Transactions on Circuit Theory, Vol. Ct-9, pp. 29-32; March 1962.